REMARKS

Claims 1-26 and 32-44 were pending in the application and were rejected, and claims 27-31 were withdrawn from consideration. Claims 1-3, 6-26, 32-35, and 37-44 are amended herein, and claims 4-5 and 36 are cancelled. In view of the following remarks, reconsideration of the application as amended is respectfully requested.

Claims 2-11, 13-19, 21-26, and 33-44 were objected to due to antecedent basis ambiguity in the preamble. The claims have been amended as suggested by the Examiner in order to overcome this objection.

The specification was objected to due to the use of bold underlined type in the section headings and title. Appropriate changes have been made above.

Claims 1-10, 12-26, and 32-41 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,827,776 ("Bandyopadhyay") in view of U.S. Patent Application Publication No. US 2002/0181523 ("Pinneo"). Claims 11 and 42-44 were rejected likewise, with the additional inclusion of U.S. Patent No. 6,479,399 as a reference. Applicant respectfully traverses these rejections, and submits that a prima facie case of obviousness is lacking.

The Examiner states that Bandyopadhyay discloses "conductive material 26(16) defining a plurality of spaced lines, opposing sidewalls of the spaced lines defining a distance therebetween less than a height of the conductive material 26(16)." Applicant respectfully disagrees. Reviewing Figure 1, which shows a top view corresponding to cross-sectional Figures 2 and 3, it is apparent that conductive material 26 is not a spaced line. Rather, as described at col. 5, lines, 35-36, material 26 comprises "contacts 26 extending between select ones of conductors 12 and 14." Continuing in the description, "placed solely within second dielectric 24 is third conductor 16." (col. 5, ll. 36-37.) Thus contacts 26 are not spaced lines with respect to conductor 16, but are merely interconnects between spaced lines on two levels. Furthermore, the whole approach of Bandyopadhyay is to avoid placing neighboring bus lines in close proximity, as his structure is taught to avoid parasitic capacitance problems by "a staggered arrangement of conductors configured at dissimilar elevational levels within an interlevel dielectric structure." (col. 2, l. 50 to col. 3, l. 3.)

Pinneo and Bandyopadhyay disclose non-analogous devices. In Pinneo, instead of an integrated circuit, a monolithic BaO substrate 42 is selected for its high thermal conductivity, allowing the operating temperature of an overlying assembled laser diode array to be reduced by channeling heat to a backplane cooler 34, which is not a ground plane as the Examiner asserts. (paragraphs 27 and 28.) Applicant fails to see any suggestion for the combination of Pinneo and Bandyopadhyay, or any way in which the references could possibly be combined.

The Examiner states that it would be obvious to have three separate drivers driving the three separate lines from the same signal "because such structure is conventional in the art for forming multilevel interconnect structure in order to have high density interconnect." Applicant respectfully disagrees that such a structure is conventional and is unaware of such a structure, and requests that the Examiner provide a reference illustrating such a structure. The Examiner's suggestion that this structure would form a high density interconnect is not understood—how do a plurality of spaced lines each driven with the same signal increase signal density?

Given the noted absence of a reference teaching multiple spaced lines driven with a common input signal, Applicant submits that each of the claims as amended is patentable. Independent claim 1 now incorporates the concepts found in original claims 4 and 5 of "a plurality of drivers, each driving the proximal end of a respective one of the spaced lines, each driver receiving a common input signal." Independent claim 12 now incorporates a similar concept: "a plurality of amplifiers to drive respective conductive lines of the plurality of conductive lines, in which the amplifiers of the plurality comprise inputs electrically coupled in common to a signal node." Independent claim 20 now incorporates the concepts fairly found in original claims 24 and 25 of "a plurality of amplifiers, each associated with at least one of the conductive lines and driving the source end of the at least one of the conductive lines, each amplifier having an input coupled to a signal node common to each amplifier." And independent claim 32 now incorporates the concept found in original claim 36 of "a data buffer to source a data signal to the plurality of conductive lines."

The claim elements noted above are neither taught nor suggested by the prior art, and therefore a prima facie case of obviousness is lacking for all claims. Applicant submits that not only is the inclusion of multiple amplifiers driving the same signal on multiple spaced lines not obvious, it goes against the general goal in semiconductor devices of reducing active

device count and line-routing space. And the stated improved results in the exemplary embodiments (improvement in propagation delays, page 3, lines 7-9; shielding a center conductor from external noise, page 6, line 20) are novel and noteworthy. The Examiner argues that the use of plural amplifiers produce "no functional differences and therefore would have been obvious"—but the specification teaches otherwise.

The dependent claims are patentable not only because they depend from patentable independent claims, but also due to additional elements neither taught nor suggested by the prior art. The Examiner argues that various dimensional ratios are obvious from the prior art. Although Bandyopadhyay certainly does not teach such ratios, it would be difficult to claim that such ratios are entirely missing from the prior art. What is missing, however, is the overall claimed device, i.e., the use of such ratios in parallel lines carrying versions of the same signal, in order to enhance signaling.

With respect to dependent claims adding dummy loads to some lines and receivers to others, Applicant disagrees with the Examiner's conclusion that such are mere design choices. The Examiner has shown no prior art motivation for including such structure, and even states a view (presumably from the Examiner's view of the art) that such appear to produce "no functional difference." As noted in the application and above, however, the overall structure improves the signaling on the conductor connected to a receiver, and the dummy loads terminate the other conductors, e.g., thereby matching impedances, controlling reflections, etc. (page 6, lines 13-32.)

In summary, Applicant submits that a prima facie case of obviousness is lacking for the active claims as amended, and respectfully requests withdrawal of the outstanding prior art rejections.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-3, 6-26, 32-35, and 37-44 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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